House Committee on Science, Space, and Technology

"Ensuring American Leadership in Microelectronics"

Testimony of Dr. Ann Kelleher

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December 2, 2021

Chairwoman Johnson, Ranking Member Lucas, and members of the Committee, thank you for inviting me to testify about the status of advanced semiconductor development and manufacturing in the United States, and to share my perspective about new federal investment and public-partnerships to support U.S. leadership in semiconductor innovation and manufacturing throughout the supply chain.

I am the Executive Vice President and General Manager of Technology Development at Intel Corporation, which is the group at Intel dedicated to advancing Moore's Law by creating new transistor architectures, wafer, and packaging processes that we turn into products for the personal computers and cloud infrastructure we are using to safely conduct this hearing, as well as for emerging technologies like 5G networks, artificial intelligence (AI), Internet of Things (IoT), and quantum computing.

Semiconductors are fundamental to U.S. technology leadership, our economy, and national security. They represent the fourth largest U.S. export sector, and the pandemic has only accelerated the adoption of digital infrastructure powered by semiconductors. Recent supply chain disruptions due to COVID-19 and widespread chip shortages illustrate the risks to our economy and the danger of losing our ability to make advanced chips in the United States.

Yet America has lost significant share of semiconductor production to Asia over the last 30 years. For decades, countries in Asia have provided substantial incentives to build domestic semiconductor champions, driving a 30 percent cost disadvantage for chipmaking in the U.S. and a corresponding decrease in U.S. share of global chip manufacturing. Since 1990, that share has dropped from 37 percent to 12 percent, and it is projected to erode further to 9 percent by 2030.

Federal investment is urgently needed to reverse this erosion by leveling the playing field for America's semiconductor industry. Almost one year ago, Congress took a critical step by authorizing new semiconductor manufacturing and R&D programs through the CHIPS for America Act. In June, the Senate approved $52 billion in appropriations for the CHIPS Act through the bipartisan U.S. Innovation and Competition Act. Now, Congress must finish the job by enacting CHIPS funding as soon as possible. Intel is doing its part to invest in American leadership by conducting the majority of our R&D and manufacturing in the United States, and we look forward to partnering with the federal government through the CHIPS Act programs to enhance domestic semiconductor R&D and manufacturing.

As the only U.S. semiconductor company with the depth and breadth of intelligent silicon, platform, software, architecture, design, manufacturing, and scale, as well as innovation and leading-edge manufacturing capabilities here in the U.S., Intel is uniquely positioned to help the U.S. regain leadership.

Executive Summary

A November 2021 paper from the Boston Consulting Group (BCG) identified the three essential ingredients for a strong U.S. semiconductor industry: i) manufacturing process technology, including intellectual property (IP) and know-how based in the United States; (ii) U.S. fab capacity to support growing demand in the U.S. and worldwide, and (iii) advanced packaging capability and capacity. BCG also identified the two most significant gaps currently facing the United States in establishing those three ingredients: (i) a 30 percent or more cost disadvantage with East Asia that U.S. chipmakers face; and (ii) public funding for R&D, which lags both Taiwan and Korea where the most advanced semiconductors are currently manufactured. Forty years ago, federal investment in semiconductor R&D was more than double that of private investment, but today, U.S. private investment is nearly twenty times that of public funding.

The U.S. government will need to effectively leverage funding from the CHIPS Act that will be allocated to new and existing R&D programs to ensure we achieve and maintain American technology leadership. To do so, the government should take an inventory of existing federal R&D programs and partnerships with private industry to identify the critical technology gaps, and with the help of the Industrial Advisory Committee established pursuant to the CHIPS Act, determine how best to fill those gaps by using existing infrastructure in combination with new resources. These efforts should be part of developing a national semiconductor strategy and technology roadmap. The two most significant new R&D programs under the CHIPS Act are the National Semiconductor Technology Center (NSTC) and the National Advanced Packaging Manufacturing Program (NAPMP).

- NSTC. Intel recommends the NSTC prioritize R&D on future breakthrough challenges that align with industry goals, and leverage existing industry infrastructure to save time and cost. NSTC should be led by a neutral non-profit that can reconcile conflicting views, such as around IP policy.

- NAPMP. High-performance chips rely heavily on advanced packaging technology, and that reliance coupled with the current worldwide capacity constraints, has highlighted the need for self-sufficient domestic packaging infrastructure. The NAPMP should establish a Package Research Center (or Centers) that allow for packaging integration – combining all the different parts together to develop and demonstrate a complete solution that improves chip performance and reduces its size.

The CHIPS Act has the right provisions to create a strong U.S. semiconductor industry, and we have confidence that if funded in a robust and sustained manner, these programs will significantly increase supply chain resiliency and contribute to American technology leadership.

Background

Intel Corporation is the world's largest semiconductor manufacturer,[1] employing over 110,000 people globally and approximately 53,000 in the United States. Intel is headquartered in Santa Clara, California and has innovation hubs in Oregon, Arizona, California, New Mexico, and Texas. Intel builds most of its product designs within its own leading-edge manufacturing and advanced packaging network, and offers foundry services for fabless chip design companies. Intel invested around $33 billion in capital expenditures and $27 billion in R&D from 2019-2021, the majority of which is conducted here in the United States.[2] Intel ranks sixth among publicly-traded U.S. companies in its individual R&D investment, and directly contributed almost $26 billion to U.S. Gross Domestic Product (GDP) in 2019, with a total GDP impact to the U.S. economy of $102 billion.[3]

Intel is making unprecedented new investments in U.S. semiconductor manufacturing capacity. Earlier this year, we announced plans to invest $20 billion in the construction of two new fabrication facilities in Arizona,[4] and to invest $3.5 billion in our New Mexico facility for the manufacturing of advanced semiconductor packaging technologies.[5] We also have announced our intention to select a new U.S. greenfield site worth up to $100 billion in investment over the next decade. These plans demonstrate Intel's ongoing commitment to leadership investments in R&D and capital expenditures in the United States, investments that enhance U.S. technological leadership and ultimately U.S. national and economic security.

Each job at Intel is estimated to support up to 13 other jobs elsewhere, meaning Intel directly or indirectly supports more than 700,000 full-time and part-time jobs in the United States.[6] Our workforce is highly educated with approximately 90 percent of people working in STEM related professions. We employ many disciplines of technical experts including engineers, chemists, physicists, and mathematicians. In the United States Intel regularly hires graduates with associate degrees, baccalaureate, master's and PhD's. In recent years on average Intel has hired over 150 students graduating from PhD programs, a significant proportion of the graduates in targeted fields across the country.

Intel is one of only three semiconductor manufacturers in the world making advanced semiconductors and the only one with its research and development anchored in the United States. The semiconductor products that Intel manufactures provide the foundations for technologies ranging from personal computing, cloud computing, artificial intelligence (AI), Internet of Things (IoT), 5G, autonomous vehicles, quantum computing, to high-performance-compute solutions, that advance humanity's understanding of, and response to, society's most pressing challenges.

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[1] See IBISWorld Industry Report 33441a, "Semiconductor and Circuit Manufacturing in the US," June 2020.
[2] See https://www.intel.com/content/www/us/en/newsroom/news/us-economic-impact-study.html#gs.0juavq.
[3] Id.
[4] See https://www.intel.com/content/www/us/en/newsroom/news/idm-manufacturing-innovation-product-leadership.html#gs.zog0za.
[5] See https://www.intel.com/content/www/us/en/newsroom/news/new-mexico-manufacturing.html#gs.0i5sdw.
[6] See https://www.intel.com/content/www/us/en/newsroom/news/us-economic-impact-study.html#gs.0juavq.

Technology Development at Intel

I lead Intel's Technology Development organization, which creates the baseline technology underpinning Intel's products and the manufacturing technology required to bring innovations into the physical world. This team's work resulted in an average of over 1,000 US patents filled per year over the last several years. I will provide a brief overview of the major teams and our process technology roadmap.

Components Research invents, develops, and demonstrates viable revolutionary and game-changing process and packaging technology options for enabling Moore's Law extension and Intel product differentiation. They then transfer those innovations and enabling technologies to other Technology Development organizations for their use in manufacturing development. This team also champions and directs over 200 university research projects annually.

Logic Technology Development is widely recognized as one of the preeminent silicon process engineering organizations in the world, consisting of approximately 8,000 employees based primarily in Hillsboro, Oregon. It produces the 'heart' of Intel products, the transistor, that is used to build a microprocessor. To maintain a predictable Moore's Law driven cadence of silicon products, at any given time, approximately four to five logic process technologies are in various stages of the development cycle, from Pathfinding to Deployment. In addition, based on strategic direction or specific product needs, two to three specialty process flows, such as advanced memory or analog/RF processes, are typically in one of the development stages.

Our **Design Enablement Group** enables both internal and external design teams to deliver winning products on Intel's cutting-edge technologies. They are responsible for delivering best-in-class Process Design Kits, which are Computer-Aided Design representations of the silicon technology to enable designs. This team also works closely with Logic Technology Development to optimize the transistor development, routing and tools, flow and methods to deliver best-in-class power, performance, and area for Intel's products. Lastly, they deliver foundational IP and test-chips and test vehicles which are a critical part of the technology development for yield and IP learning.

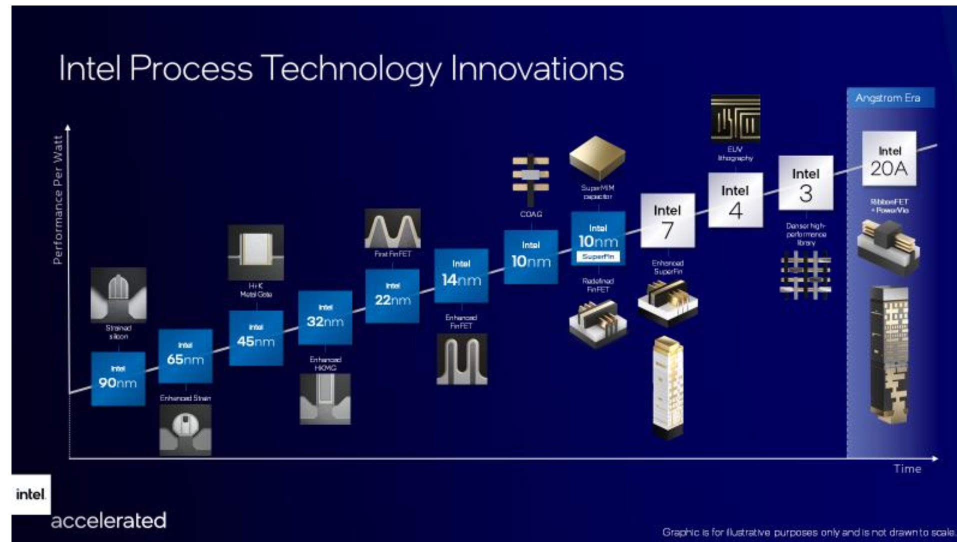
The **Assembly Test and Technology Development Group** is the world leader in advanced packaging technologies with a strong portfolio of 2.5D and 3D advanced packaging offerings. This team has substrate and assembly factories to develop leading edge packaging technologies. They create industry-leading known good die sort and test capability, and they offer package design services and silicon package co-design enablement and offer world-class board assembly.

Intel's Process Technology Roadmap

Earlier this year, I helped unveil one of the most detailed process technology roadmaps that Intel has ever provided, showcasing a new node naming system and breakthrough technologies that will power new products through 2025 and beyond, including:

- **RibbonFET**, our first new transistor architecture in more than a decade
- **PowerVia**, an industry-first new backside power delivery method

- **High NA EUV**, our plans to adapt next-generation High Numerical Aperture extreme ultraviolet lithography



Intel's technology roadmap relies on new levels of innovation, including not only deep transistor-level enhancements, but also innovations all the way up the stack to the interconnect and standard cell level. The company has moved to an accelerated pace of innovation to enable an annual cadence of process improvements.

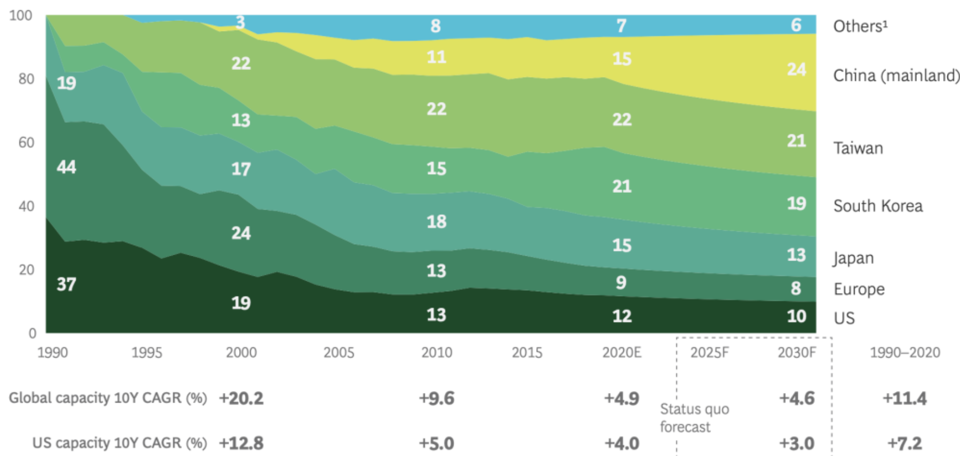
Manufacturing at Intel

While Intel conducts the majority of manufacturing in the United States, our global manufacturing scope and scale enable us to provide our customers with a broad range of leading-edge products. Integrated manufacturing has been foundational to our success, enabling product optimization, improved economics, and supply resilience. As semiconductor manufacturing becomes more complex, Intel is one of the few remaining firms in the world, and the only one in the United States, that can do both leading-edge design and manufacturing in-house.

Intel has nine global manufacturing sites—five for silicon wafer fabrication and four for the assembly and testing of our products. We operate in a network of manufacturing facilities integrated as one factory to provide the most flexible supply capacity. Our new process technologies are transferred identically from our central development fab in Oregon to each manufacturing facility. After transfer, the network of factories and the development fab collaborate to continue driving operational improvements. This enables fast ramp of the operation, fast learning, and better quality control.

State of U.S. Semiconductor R&D and Manufacturing

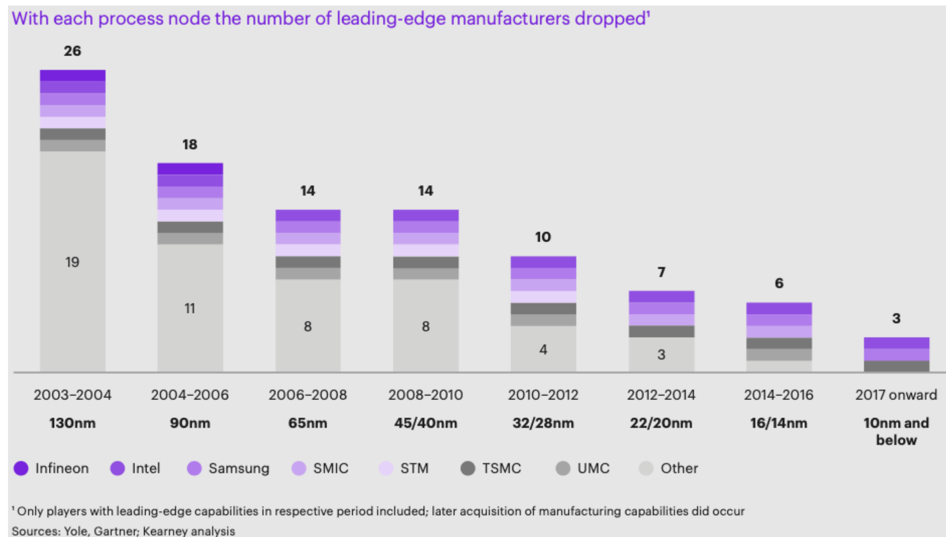
The U.S. share of semiconductor manufacturing capacity has experienced a precipitous decline over the last 30 years. In 1990, the United States represented 37 percent of the world's supply of semiconductors but today comprises only 12 percent, a share forecasted to decline even further without intervention.[7] In contrast, Asia is now home to about 75 percent of the world's total semiconductor manufacturing capacity. This imbalance exists mostly because foreign governments have invested heavily in chip manufacturing incentives while the U.S. government has not.



Designing and manufacturing leading-edge chips has become increasingly costly at each node size. The capital expenditures required to build and outfit a leading-edge fab have grown exponentially from around $3 billion just a decade ago to $20 billion today. Substantial investments into process

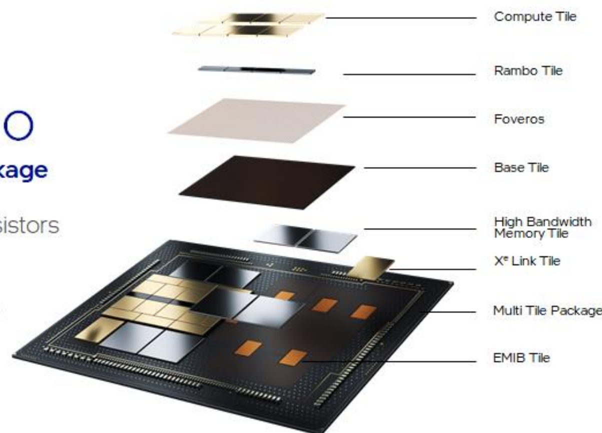
[7] See https://www.semiconductors.org/resources/sia-summary-of-bcg-sia-report-government-incentives-and-u-s-competitiveness-in-semiconductor-manufacturing/

technology development are also necessary to master the processes required to operate a leading-edge fab, but integrated circuit scaling is getting more difficult as traditional devices reach their scaling limits. As a result, lithography is now the most important step in fabricating integrated circuits and is also the most expensive in terms of total wafer processing cost. Due to these dramatic increases in manufacturing and technology development expenses, fewer and fewer manufacturers globally can absorb the investments required to develop the latest node sizes (see figure below).[8] Today, only three leading-edge logic manufacturers remain: Intel, Samsung, and TSMC.



Advanced packaging technologies are also undergoing a major transition from primarily connecting small geometry wiring on a die to the looser wiring density on system board to connecting small geometry wiring between many die inside one package. This 3D Heterogeneous Integration, using novel package technology as its core building block, is becoming vital to the semiconductor industry as traditional chip scaling slows down. Currently, less than two percent of the capacity for assembly, test and substrate manufacturing is in the United States. With the reported investments of Asian countries coupled with that of Asian private sector companies in 3D packaging, the United States and U.S. based companies are becoming further challenged to maintain their leadership.

[8] See https://www.kearney.com/communications-media-technology/article/?/a/europes-urgent-need-to-invest-in-a-leading-edge-semiconductor-ecosystem.



Intel's Ponte Vecchio, a product targeted for Argonne National Laboratory's exascale Aurora Supercomputer, represents the current state of the art in packaging.

A November 2021 paper from the Boston Consulting Group (BCG) identified the three essential ingredients for a strong U.S. semiconductor industry: 1) U.S. fab capacity to support growing demand in the U.S. and worldwide, 2) advanced packaging capability and capacity, and 3) manufacturing process technology including IP and know-how based in the United States.[9] BCG also identified the two most significant gaps currently facing the United States: the 30 percent cost disadvantage faced by chipmakers domestically and public funding for R&D which lags both Taiwan and Korea. Forty years ago, federal investment in semiconductor R&D was more than double that of private investment ($1 billion federal to $0.4 billion private). But today, private investment is nearly $40 billion, vastly exceeding the federal government investments of $1.7 billion in semiconductor-specific R&D and $4.3 billion in research in semiconductor-related fields."[10]

Federal government support for both R&D and manufacturing is needed to address these gaps and maintain a world-leading U.S.-based semiconductor industry. The CHIPS for America Act enacted in the National Defense Authorization Act for Fiscal Year 2021 established an effective framework of federal programs and public-private partnerships to address R&D and manufacturing challenges, including the following:

- **Financial Assistance Program** to incentivize investment in facilities and equipment for semiconductor fabrication, assembly, testing, advanced packaging, or R&D,
- **National Semiconductor Technology Center** (NSTC) public-private consortium to conduct research and prototyping of advanced semiconductor technology,
- **National Advanced Packaging Manufacturing Program** to strengthen domestic semiconductor advanced test, assembly, and packaging capability, and

[9] See https://www.bcg.com/publications/2021/establishing-leadership-in-advanced-logic-technology
[10] See https://www.semiconductors.org/sparking-innovation/

- **Industrial Advisory Committee** to advise the federal government on matters relating to microelectronics R&D, manufacturing, and policy.

These programs must be funded by Congress as soon as possible so that implementation can begin. Other countries in Asia and the EU are doubling down on their existing investments in semiconductor development and manufacturing, and the United States risks being left further behind.

National Semiconductor Technology Center (NSTC) Recommendations

Intel has been working with many groups including The Semiconductor Alliance to make recommendations for the NSTC. MITRE Engenuity, a non-profit arm of MITRE, and The Semiconductor Alliance recently developed and published a white paper to address the challenges of bridging the valley of death and driving innovation.[11] Intel supports the group's vision, which outlines how a carefully planned NSTC will address key challenges for the semiconductor industry:

- **A Marketplace of Competitive Ideas –** Launch Breakthrough Challenges that align industry around revolutionary goals that result in competitive products manufactured in the United States.
- **A Whole-of-Nation Effort –** Leverage and develop access to a nationwide network of existing facilities at U.S. companies to save cost and time.
- **High-Impact Investment and Incubation –** Establish an investment fund that fills emerging companies' need for capital and connects companies with resources and facility access to de-risk technology maturation.
- **A Workforce of the Future –** Invest in a robust domestic semiconductor workforce through curriculum development, internship and job opportunities, scholarships, vocational training programs, and K-12 educational resources.
- **Neutral, Balanced, and Resilient Governance –** Create an effective governance model that mitigates conflicts of interest and remains focused on the good of the nation and the U.S. semiconductor industry.
- **Accountability to U.S. Government Objectives –** Coordinate with existing and future U.S. government programs.

Intel also believes the following key guiding principles are critical to the NSTC's success:

- **Governance Framework** – 1) Should be led by a neutral non-profit, not a member of the industry, 2) should be focused on the needs of U.S. semiconductor manufacturers and their key suppliers, and 3) should not include foreign semiconductor manufacturers as a part of the governance.
- **Funding** – Should come from both the federal government and participating U.S. companies, prioritize U.S. companies' R&D leadership, focus on revolutionary research projects targeted for 6-12 years out, and must enable long-term sustainment of the NSTC.
- **Prototyping Projects** – Best done 1) by one leading U.S. company with invited participation from key suppliers or research groups, 2) in a U.S. company's facilities for cost and efficiency

[11] American Innovation, American Growth: A Vision for the National Semiconductor Technology Center, MITRE Engenuity, November 2021, available at https://info.mitre-engenuity.org/semiconductor-alliance-vision-for-nstc

benefits, and 3) may include research partners from other companies or universities at the discretion of the lead company, but results are considered proprietary.

- **IP Policy** – Intellectual property (IP) should be owned by the companies doing the research, not by NSTC, and pre-competitive research can be collaborative multi-company projects.

In the semiconductor industry, breakthrough technologies can take over 10 years to become commercially marketable, manufacturing fabs cost tens of billions of dollars, and technical risk is high. Without investment, many ideas have no domestic path from “lab to fab.” Funding, while critical, is not the only thing that companies need to shepherd new technologies across the valley of death. It is equally critical to have access to facilities, tools, and personnel suitable for demonstrating the ability to produce an innovation at commercial scale. While some prominent market leaders like Intel have their own corporate facilities for prototyping and scaling novel technologies, they tend to be the exception rather than the rule, and these facilities are typically not accessible to external teams.

National Advanced Packaging Manufacturing Program Recommendations

The rapid proliferation of high-performance products that rely on advanced packaging technology, coupled with the current worldwide capacity constraints, have highlighted the need for a robust, self-sufficient domestic infrastructure ranging from research through development to production. A critical imperative to meet these challenges and the requirements of the National Advanced Packaging Manufacturing Program is to establish a Package Research Center (or Centers) that allows for packaging integration – combining all the different parts together to develop and demonstrate a complete solution that improves performance and reduces size. This integration should span the complete ecosystem – from manufacturers to customers, from university researchers (faculty and students) to staff from the industrial sector, from material suppliers to equipment suppliers, from software providers to hardware providers.

With the establishment of a dedicated center for advanced assembly, test, and substrate development, basic integrated flows can be demonstrated, and prototypes built that meet key performance and quality and reliability metrics and enable rapid scaling in a domestic based manufacturing base. A center would provide a location for participants from academia, U.S. companies and the U.S. government to work together to develop leadership technologies and an educated and highly capable work force to support an innovative and robust domestic packaging industry. In Intel’s discussions with many universities and with industrial partners, there is a strong consensus to establish this type of joint development center, which would build on the multi-tiered programs and projects where Intel collaborates across the ecosystem.

In addition, a Package Research Center should develop next generation substrate technologies that continue to support Moore’s Law requirements and the development of heterogeneously integrated micro-systems. Package substrates are currently manufactured overseas, which puts our supply chain at risk. A Package Research Center could explore cost-effective manufacturing techniques to enable package substrates to be domestically manufactured and integrate advanced smaller geometry higher performances substrate technologies with assembly and test technologies.

Workforce Perspectives

Ensuring U.S. leadership in semiconductors also requires a reliable workforce, including workers with advanced degrees in STEM fields and other highly trained technical workers. Fewer U.S. students, however, are choosing the semiconductor industry as a career choice, which threatens to make workforce availability a limiting factor to a strong U.S.-based semiconductor industry. Approximately 90 percent of Intel's employees work in STEM-related technical roles—from engineering, physics, and chemistry to cooling, filtration, and technical maintenance. Filling new jobs in each of these fields, especially at a time when competition for technology workers is only intensifying, presents additional challenges that we cannot fully address on our own.

More government assistance—at the federal, state and local level—is needed to address shortfalls in the STEM talent pipeline, including the longstanding gaps in access to STEM education and training that have been magnified by the global pandemic. Government and industry must partner together to both expand educational/training opportunities and increase interest in STEM fields. Particular attention needs to be focused on females and students from low-income communities who continue to be underrepresented in the STEM pipeline.

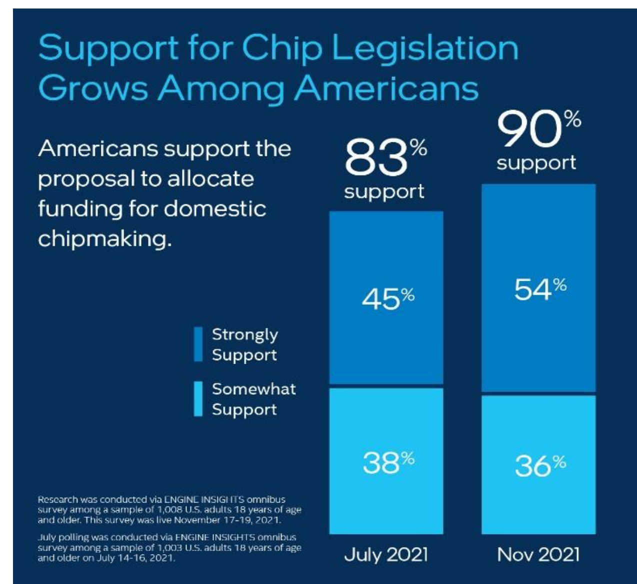
We must also work together to significantly increase access to, and participation in, STEM-related higher education—from technical training to post-doctoral research. Efforts must be made to increase and scale scholarships in engineering, computer science, and other critical STEM fields, as well as graduate research fellowships and post-doctoral programs. We must also provide additional support to community colleges, vocational institutions, and other entities that educate and train individuals in related technical disciplines. Such entities include the U.S. Armed Forces, where Intel has found success in recruiting experienced individuals for technical roles in our fabs.

Relatedly, we know that we will never solve the shortage in STEM workers without a specific focus on underrepresented minority groups. One successful model is the **National GEM Consortium**, which is already supported by the NSF and has helped to increase diversity in the STEM workforce. Through the program, Intel supports minority students seeking graduate STEM degrees—including through financial assistance, internships, and mentorship—often leading to successful careers at Intel. NSF support can benefit similar collaborative programs, including partnerships with Historically Black Colleges and Universities (HBCUs) and other minority-serving institutions. In 2017, for example, Intel launched a $4.5 million program with six HBCUs to increase participation in electrical engineering, computer engineering, and computer science. These partnerships have yielded results – for example, at Howard University, enrollment in computer science and computer engineering has increased by 55 percent and 47 percent, respectively. With government support, potentially through the NSTC, these and similar programs could reach many more students to help bolster the domestic semiconductor industry workforce.

Call to Action on CHIPS for America Act Funding

The CHIPS for America Act offers a vital course correction for the United States which will provide essential domestic semiconductor capacity and act as a counterbalance to the policies of other countries designed to concentrate global chipmaking in East Asia. Intel supports robust funding from Congress as soon as possible to implement the CHIPS Act's semiconductor manufacturing and R&D programs. Time is of the essence: American businesses in every sector across the economy are facing a semiconductor shortage, and the only way to alleviate the current supply-demand imbalance long term is to increase manufacturing capacity by funding and implementing the CHIPS Act.

Recent nationwide polling of Americans indicates an understanding of the importance of the chipmaking industry to the U.S. economy and national security, and widespread support for Congressional action to allocate federal funding for the industry.



This Committee has an important oversight role regarding many of the CHIPS Act programs, and Intel looks forward to working with you to provide our perspective on implementation of these programs going forward. Thank you for holding this important stakeholder hearing, and I look forward to answering your questions today and working with you to advance U.S. semiconductor manufacturing and R&D.

Ann Kelleher Biography

Dr. Ann B. Kelleher is Executive Vice President and General Manager of Technology Development at Intel Corporation. She is responsible for the research, development and deployment of next-generation silicon logic, packaging and test technologies that power the future of Intel's innovation.

Previously, Dr. Kelleher was General Manager of Manufacturing and Operations, where she oversaw Intel's worldwide manufacturing operations including Fab Sort Manufacturing, Assembly Test Manufacturing and strategic planning, as well as corporate quality assurance and corporate services. Before that, she served as co-general manager of the Technology and Manufacturing Group.

Dr. Kelleher joined Intel in 1996 as a process engineer, going on to manage technology transfers and factory ramp-ups in a variety of positions spanning 200mm and 300mm technologies. She started her manufacturing leadership journey as the factory manager of Fab 24 in Leixlip, Ireland. She has also been the site manager of Intel's Fab 11X fabrication facility in Rio Rancho, New Mexico, and plant manager of Intel's Fab 12 facility in Chandler, Arizona. She then became General Manager of the Fab Sort Manufacturing organization where she was responsible for all aspects of Intel's high-volume silicon manufacturing.

Dr. Kelleher holds a bachelor's degree, a master's degree and a Ph.D. in electrical engineering, all from University College Cork in Ireland.